

KAWASAKI STEEL TECHNICAL REPORT

No.27 ( November 1992 )

Hot-Rolled, Cold-Rolled and  
Surface Coated Steel Sheets  
and Electronics and Instrumentation

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Image Processing System with a New Systolic Array LSI

Akira Ichinose, Kenji Suzuki, Yoshinori Wakimoto, Mitsuru Yanagisawa, Yuichiro  
Asano

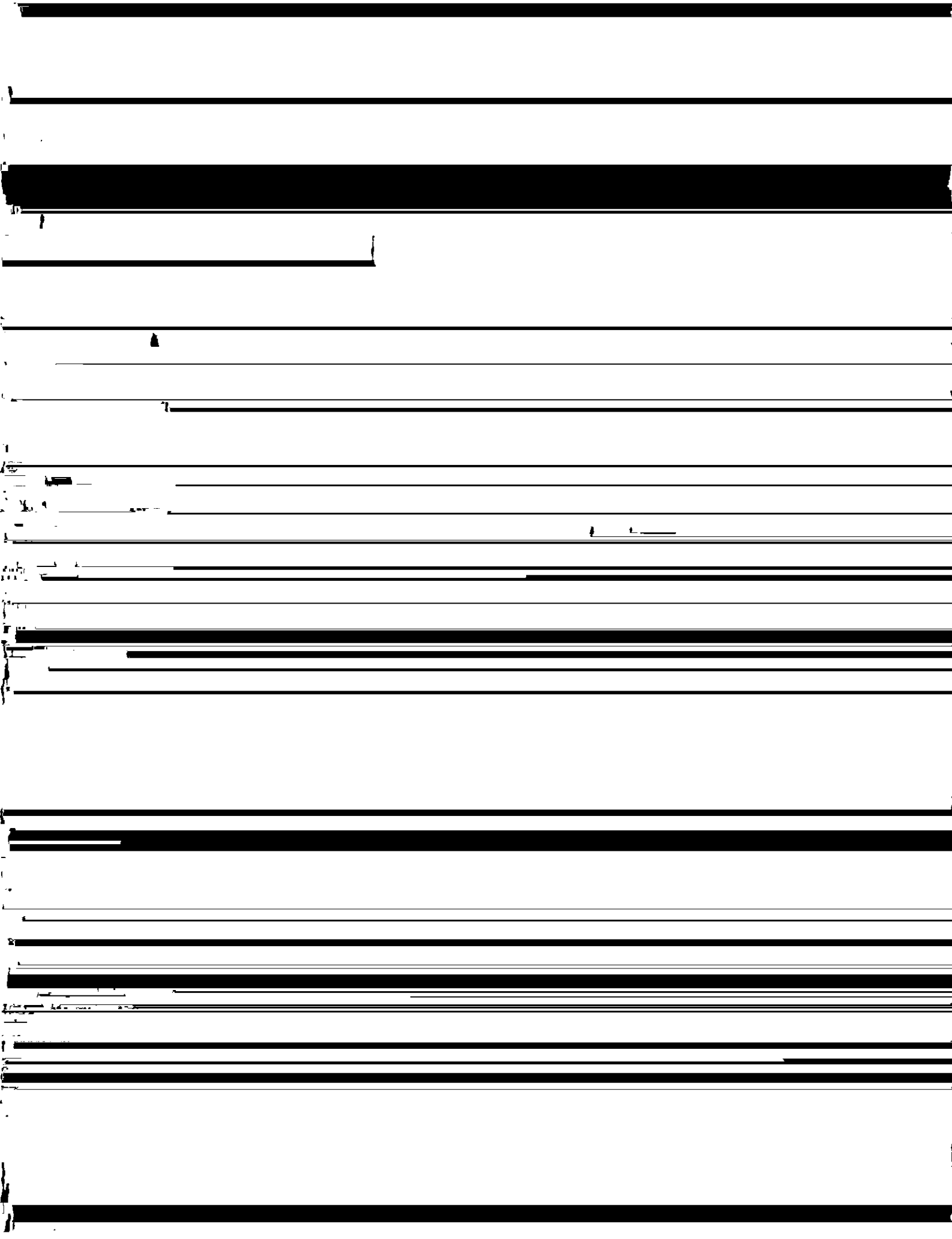
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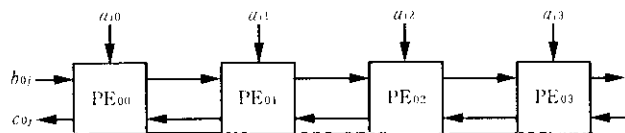
Synopsis :

# Image Processing System with a New Systolic Array LSI\*

*Synopsis:*

*Abstract:*





user of an image processing board employing such an LSI can obtain high performance, until the limit of the array size is reached. Once this limit is exceeded, however, performance suddenly drops. As a result,

Table 1 LSI function list

previous processing. The processing proceeds as follows:

(1) The image data are read from a memory block;

Two-dimensional convolution

(2) the image data are processed by the convolution operation;

Matrix-vector multiplication

array to carry out the convolution operation; (4) the

Gray scale transformation with look-up table

output level is adjusted by the parallel shift register.

Table 2 Performance comparisons—image processing time for convolution of  $512 \times 512$  8-bit

Kernel Size	Iterations	Time (ms)	Time (ms)	Time (ms)	Time (ms)
$3 \times 3$	2000	6.6	13.1	13.1	6.6

a WS, control is transferred to Dr. IMAGE II. The LSI  
not be considered as a unit for serial processing in the

Table 3 Hardware component function list

tical, the architecture could be simplified and independent operation of Dr. IMAGE II became possible. Communication between the WS and Dr. IMAGE II are

Dr. IMAGE II, which has the following features:

- (1) The image size and kernel size are variable so that a

large image size can be 4,000 x 4,000 pixels.