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Content Addressable ROM with a Variable Length Match Function–CAROM*

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1. Introduction

The cycle time for each mode is 120 ns (**Fig. 1**).

figured in 16 bits, and a function is added to connect adjacent words. In addition, each word is provided with a match flag to indicate if it matches external data obtained in the data retrieval mode.

3 Operation

Figure 3 shows an example of operation. Consecutive addresses are loaded with X, Y, and 123. The first two

this data to look up other memories, data with respect to X and Y is provided instantaneously. Needless to say, it also becomes possible to use a "don't care" function in a bit unit at the time of retrieval and sequentially output multiple match addresses at the time of match address output.

4 Applications

are names called X and Y, and 123 to follow is a memory address in which reference data is stored.

In the retrieval mode, continuous search with two data X and Y completes a comparison and matching of all stored data in only 2 cycles and, in the end, a hit flag is set on the i-th Y word.

Then, in the address match mode, inputting a read pulse outputs the i address of the "Y" word. By incrementing the i address by one with the CPU and looking

High-speed content addressing of re-loadable memories is used for a high-speed addressing circuit in advanced microprocessors. In addition, a few other application examples have been reported.[2-4] However, the LSI reported here is the first high-speed LSI with large-scale integration for fixed data, which is also capable of handling data with variable length.

The CAROM, as a future fixed data storage element, is considered to have promising applications in the field